A New Method for Path Criticality Calculation

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***Abstract*—Technology scaling and manufacturing process affect the performance of digital circuits, making them more vulnerable to environmental influences. Some defects are manifested as delay faults. Some various factors have impact to signal propagation delay. A new method is presented for determining factors impact measurement on the path delay in the digital circuits. The method is focused to find the best weights of the factors used as parameters for the PaCGen (Parameterized Critical Path Generator) system. PaCGen is used for critical paths selection based on static timing analysis data with impact of factors to propagation delay. Experimental results are provided using the ISCAS'89 benchmark circuits.**

Keywords—delay fault testing; path delay fault; critical paths; criticallity calculation

I. INTRODUCTION

Recent advances in new technologies have resulted in increasing digital circuits' complexity and reducing their physical dimensions. Higher clock frequencies and technology scaling cause degradation of digital circuits due to process variations and manufacturing defects.

Defects in digital circuits are modeled by faults that are generally described as inability to perform a circuit function defined in design specification. Faults affecting time performance of digital circuits are called *delay faults*. Several delay fault models exist and are used in digital circuits testing from which a path delay fault model is more important based on its complexity.

The path delay fault represents the cumulative delay of a combinational path to exceed some specified duration. A combinational path begins at a primary input or at the output of a clocked flip-flop, contains a connected chain of gates, and ends at a primary output or at the output of another clocked flip-flop. A propagation delay is the time that a signal event takes to traverse the path [1]. The number of paths in the circuit increases exponentially with its size. Therefore the path delay fault model is usually applied on a small portion of selected critical paths to generate the test set for them. The critical paths are functional circuit paths with small timing slack necessary for the proper signal transition propagation [2]. The slack is a time margin which is left on a tested path for proper propagation of logical values transition.

The path delay is affected by many factors which may cause either speed up or slowdown of signal propagation in the circuit. Some factors result directly from the physical implementation of the digital circuits, such as the number of layers used or circuit aging, which allow the formation of secondary parameters such as power supply noise and voltage drop in certain parts of the circuit or crosstalk effect between adjacent wires. The amount of delay is also affected by ambient temperature and used delay faults testing method. In this case, there has to be taken into account multiple inputs switching, signal transition type and test vectors used. All these factors can affect path delay alone or in a combination.

II. FACTORS INFLUENCING THE PATH DELAY

Some existing and published factors with their impact to signal propagation delay were identified [3-11] and they are shortly described in this section.

A. Number of layers

Integrated circuits can be divided into single-layer and multi-layer ones. Multi-layer integrated circuits have been proposed as a solution to the growing delays on wires due to the technology scaling. Connections between layers are realized with a through-silicon vias (TSV) filled with a conductive material. Incomplete filling of connections can cause an increased resistance on wire, thereby contributing to an increase in the overall circuit delay. The final number of layers affects the amount of the delay, since each the TSV adds some delay to the signal propagation. The biggest difference in the amount of the delay occurs between the single-layer and two-layer circuits. With more layers, the amount of additional delay gradually decreases [3].

B. Aging

Aging is one of the most important reliability concerns in nanometer technology due to introducing a significant delay in the digital circuit over time. One of the main causes of transistor aging is the Bias Temperature Instability (BTI), which gradually increases a threshold voltage of the transistor, and thereby the circuit delay. The BTI-induced delay degradation rate of the transistor depends on several causes, such as the effects of process variations and workload and operating conditions that affect the temperature and voltage profile droop. Therefore, to accurately predict aging-induced path delays, the effects of all these phenomena on circuit timing must be considered [4].

C. Power supply noise

Modern technology allows placing more transistors per chip and also increasing their operating frequency causing an increased current density and voltage drop along the supply networks. Power supply noise can be derived on the basis of inductive or resistive parameters or their combination. Inductive noise depends on the inductance and immediate current change, resistance noise is referred to as IR drop parameter and depends on current and distributed resistance in the supply network. Another important fact is the components layout on a chip, in particular a location of switching gates, which creates different hot spots and the power supply noise levels around the critical path in every circuit [5].

D. Multiple input switching

This phenomenon arises when several logic gates inputs change their value in close time proximity. Static timing analysis (STA) assumes that the logical value of only one input is changed at a time, while others maintain a stable value. This can cause problem when testing delay faults. Multiple input switching can generate significant differences in the supply network, which are known as the power supply noise, and with higher switching activity the impact on the circuit delay is much greater [6].

E. Crosstalk

Due to continuous technology scaling, the distance between interconnecting wires is reduced, which allows to form a parasitic coupling capacitance between them causing crosstalk effects and impacting the circuit delay characteristics and performance [7]. Unfortunately, it is impossible to accurately analyze the crosstalk effects without test pattern information, because there is no way to count how many aggressors affecting the critical path delay with active coupling capacitance [2].

F. Temperature

Chip temperature is affected by the dissipated power which depends on the thermal conductivity. Power dissipation hence leads to global temperature variations as well as local fluctuations in regions of high-activity. An increase in the temperature typically causes a circuit to slow down due to reduced carrier mobility and increased interconnect resistance [8]. However, this assumption fails for low voltage applications because the delay can decrease with increasing temperature values due to competitiveness between the mobility and the supply voltage. This phenomenon is known as inverted temperature dependence [9].

G. Signal transition

In older technology, logic gates were designed to have symmetrical rising and falling transitions, which led to larger cells and impaired the size of the design. Starting from 130 nm technology, logic gates need not necessarily observe this symmetry so rising or falling transition delay may be different, which can cause an additional delay [10].

H. Test vectors

Test vectors consist of a certain number of bits. This factor represents the number of undefined logical values in test vectors − X and X ∈ (0,1). When test vectors have a large number of X values, it is possible to apply test compression techniques. The compressed test set can decrease the multiple inputs switching in dependence on logical values 0 and 1 assigned to X. The paths activated by such test vectors should produce less power and the test should be robust. Results of adjusting the values of bits containing the undefined values can achieve reduction of other factors. Factors, as multiple input switching, power supply noise effect, and signal transition types, can be adjusted by using the appropriate test vectors [11].

These factors have been specified as parameters for criticality calculation of the paths in digital circuits. Each parameter has different impact to the delays, and therefore some weights for them have to be specified and involved in the expression for criticality calculation. The next section describes the new method for finding weights for the parameters.

III. A NEW METHOD FOR CRITICAL PATHS SELECTION

The additional delay caused by the influence of multiple factors simultaneously is not equal to the sum of their individual delays. This is due to interdependencies between them e.g. test vectors can increase the switching activity that leads to a higher power supply noise. All dependencies are shown in Fig. 1. The range interval of impact to the signal propagation delay for each factor is presented in Table I. These values were determined by a weighted average of the measured values from experimental results described in [3-11] omitting the smallest and the largest values. Final values were rounded to one decimal place. The process of determining the values was also affected by a number of studies in which the authors have presented similar results. These values were accepted for a newly presented method.

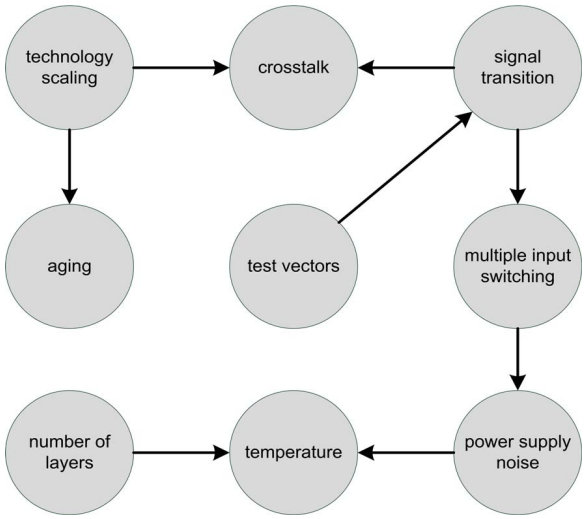

Fig. 1. Dependancies between factors influencing the path delay

TABLE I. INTERVAL RANGE FOR FACTORS

Factor Name	Interval range [%]
Number of layers	3,4 - 7,2
Aging	7,7 - 17,3
Power supply noise	10,0 - 19,0
Multiple input switching	8,7 - 18,2
Crosstalk	2,0 - 36,5
Temperature	3,0 - 5,0
Signal transition type	6,8 - 14,0
Test vectors	7,0 - 15,2

Generally, the critical paths can be specified by the static timing analysis (STA) or statistical static timing analysis (SSTA) and others. The new method has been developed for selecting the critical paths based on path criticality calculation using in the PaCGen system [12]. The influence of each factor can depend on the used technology, therefore it is necessary to develop a new method for estimation of the weights for these factors. Every path has a different kind of sensitivity to various factors, and therefore path weights have to be specified. A basic list of critical paths for the tested circuit is generated based on the STA information. They are ordered by their delay size. Then new delay values are calculated using the formula below for each critical path [12]:

$$c_p = \left(1 - \frac{S_p}{t}\right) \cdot \prod_{j=1}^{k} \left(1 - w_j\left(1 - i_{jp}\right)\right) ,$$

where:

c_p – criticality value of the path,

s_p – slack time of path from STA data,

t – time length of one clock period,

k – number of parameters,

w_j – weight (impact) of parameter,

i_{jp} – calculated impact of parameter (sensitivity to the factor).

Recommended intervals of weights for individual factors are defined and included into the PaCGen system. The developed method is focused to find the best values for these weights using the delay fault coverage of transition faults. The resulting path delays are re-ordered according to the path criticality. The new recommended ranges for weight values are presented in Table II. These values have been derived from the values shown in Table I using a condition that the weights sum does not exceed 20 %. The condition was determined in the PaCGen system [12]. Therefore, the interval values were multiplied by a coefficient to suit the given condition, while maintaining the same ratio between them. Temperature and aging factors are not involved in the analyzed factors in the PaCGen system and they are also not used in the experimental results.

TABLE II. RECOMMENDED WEIGHT OF PARAMETERS

Parameter	Recommended weight [%]
X-Filling	1,8 - 3,8
Power Supply Drop	2,6 - 5,1
Multiple input switching	2,4 - 4,4
Power consumption	0,4 - 1,0
Area overhead	0,3 - 0,7
Type of edge	1,4 - 2,6
3D	1,2 - 2,4
Sum	**10,1 - 20,0**

IV. EXPERIMENTAL RESULTS

Experimental results were provided over selected ISCAS'89 benchmark circuits [13] with 45 nm CMOS technology. The delay fault coverage using the transition delay fault model was used for evaluation of the developed and implemented method. The delay fault coverage was calculated for all possible combinations of the weights at the recommended intervals and the maximum coverage was found. The achieved results and improvements in comparison with the previous method are presented in Table III. The new method has been integrated in PaCGen. The first column describes circuits and the second one shows the number of paths selected to demonstrate the limited test length. The third column shows the delay fault coverage of the previous method when weights of parameters were set intuitively [14]. The fourth column presents the delay fault coverage achieved by the proposed method when all combinations of weights intervals from Table II were investigated.

TABLE III. DELAY FAULT COVERAGE

Circuit	# paths	Previous method [%]	Proposed method [%]	Improvement [%]
s27	44	73,8095	76,1905	2,3810
s298	369	71,5580	75,5435	3,9855
s344	568	69,8758	74,5253	4,6495
s349	584	68,5294	73,9521	5,4227
s382	640	65,2439	67,3780	2,1341
s386	331	87,5358	87,6791	0,1433
s400	716	61,2637	64,9725	3,7088
s420	590	82,2917	82,4405	0,1488
s444	856	66,9421	75,5165	8,5744
s510	590	87,4454	91,0870	3,6416
s526	656	73,2033	77,0021	3,7988
s526a	521	54,9485	57,3196	2,3711
s641	2232	55,2749	60,0297	4,7548
s820	393	51,4049	52,3627	0,9578
s832	404	50,7472	52,4284	1,6812

Circuit	# paths	Previous method [%]	Proposed method [%]	Improvement [%]
s838	807	32,0896	32,0896	0
s953	369	33,6761	33,8689	0,1928
s1196a	2478	43,3874	46,2031	2,8157
s1238	1708	33,3884	35,6198	2,2314
s1488	153	24,8775	25,1924	0,3149

V. CONCLUSION

The paper presents a new method for specification of weights of some factors influencing delay in digital circuits. The issue of the proper estimation impact of various factors on the path delay in digital circuits is a complex process due to the existing interdependencies between them, their dependencies on circuit structure and the fact that some of the factors may be changed over time. Experiments over the selected benchmark circuits show that the presented method achieved slightly better results in delay fault coverage than the previous one. Future works will be aimed at improving the proposed method to use more critical paths that should lead to more accurate results. This method will be also applied to other benchmark circuits for its effectiveness evaluation.

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