

Minimization and Partitioning Method Reducing Input Sets

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Abstract

The article describes a new Boolean minimization and single-level partitioning method based on the BOOM minimization system [6]. The minimization is performed with respect to the restrictions stated for the number of inputs and outputs of individual components and/or with the goal to reach load balancing for the inputs. The method can handle extremely large functions (up to thousands of input variables) in a very short time and its use is advantageous above all for highly unspecified functions, where the number of don't cares is large.

1. Introduction

When designing logic circuits we often encounter constraints following from the properties of the available physical elements. Whether we compose a circuit of simple logic gates, PGAs or LUTs in FPGAs, the number of inputs and outputs of one element is limited. The number of logical levels may be limited too, above all due to the propagation delay constraints. These requirements can be met by circuit decomposition. The common two-level minimization algorithms based on the Quine-McCluskey approach, like e.g. ESPRESSO [7, 9], do not support any decomposition features and the decomposition is done independently, as a sort of post-processing [10, 11]. The decomposition is then more difficult to do and the results are usually less satisfactory. Our algorithm combines these two phases to produce better results.

The problem to be solved here is a single-level decomposition of a combinational Boolean function. The resulting circuit has thus the two-level structure. The idea is illustrated by Figure 1, where the logic function of 7 inputs x_1 - x_7 and 6 outputs y_1 - y_6 is decomposed into two 5-input and 3-output blocks while each block is a two-level (AND-OR) circuit.

The input of our algorithm is a Boolean PLA matrix [7] defining the on-sets and off-sets (optionally don't care sets) of the output functions. The algorithm assigns these outputs to individual functional blocks (see Figure 1) and minimizes each set as a sum-of-product (SOP) expression according the decomposition.

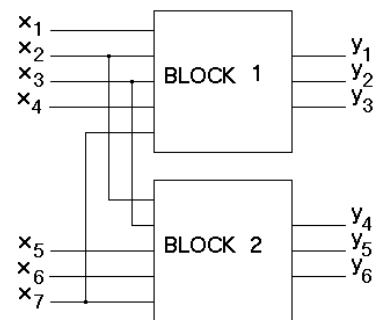


Figure 1. A single-level decomposition

In some cases not all input variables used in the input form are needed to produce the required output values. Similarly, some input variables can be substituted by others while preserving the required function. For example, in Figure 1 only five of seven input variables are needed to produce each bundle of three outputs. In this case the circuit can be decomposed into stand-alone two-level blocks. The partitioning is based on finding the minimum of input variables needed to produce a group of output functions. First the outputs are assigned to the blocks and then the minimization is performed while trying to match the maximum allowed number of inputs into the blocks.

Principles of the BOOM Approach

The suggested partitioning algorithm is based on the BOOM minimization tool presented earlier [1-5]. It consists of two major phases: generation of implicants (prime implicants for single-output functions, group implicants for multi-output functions) and the subsequent solution of the covering problem (CP). The generation of implicants for single-output functions is performed in two steps: first the Coverage-Directed Search (CD-Search) generates a sufficient set of implicants needed for covering the source function and then the implicants are expanded into prime implicants. In addition to it, for multi-output functions the primes are reduced into group implicants and then the group CP is solved. More details concerning these procedures can be found in [2,4].

We can see that using the simple CD-search and simple CP solution (upper left corner), we obtain a solution in which almost every input wire enters all blocks. By increasing the partitioning forces we reduce the number of inputs into blocks down to 98 (lower right corner) where every input enters in the average two blocks. Thus we can conclude that both partitioning forces are important, whereas modifying only the CD-search or CP solution algorithm does not produce sufficient results. Higher penalization values than those shown in the table proved to be inefficient. The solution time depends above all on the penalization of the CD-search, whereas the penalization of the CP solution algorithm does not affect the runtime.

A simple modification of this algorithm enables us to control the load distribution of the outputs of the preceding blocks, because inputs entering more than one block (branching inputs) are more loaded than those entering only one block. When input variables contained in other blocks are even more penalized, the occurrence of branching inputs is reduced and the output load of previous blocks is more balanced.

The decomposition algorithm was tested on several problems. Thus, e.g., a function with 100 inputs, 20 outputs and 100 minterms with defined output values was decomposed into 5 blocks, each having 4 outputs. The algorithm gave the following solutions. For a simple minimization all inputs were used and the average number of inputs into one block was 75. When the decomposition was performed, the number of inputs used was 58 and the average number of block inputs was 17. When the load balancing was used, the total number of inputs used was 80 and only 4 inputs were branching in contrast to 20 branching inputs in case of a decomposition without load balancing.

Conclusions

It was shown that combining the partitioning of a function with its minimization leads to better results than performing each of these design tasks independently. The modification consists in introducing partitioning forces into two phases of the minimization algorithm denoted as CD-search and CP solution. The effect of these forces on the quality of solution of a typical example was investigated and documented by a table of results.

Further research will be directed towards multi-level decomposition and the applications in the area of low-power devices.

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References

- [1] P. Fiser, and J. Hlavicka, Efficient Minimization Method for Incompletely Defined Boolean Functions, Proc. 4th Int. Workshop on Boolean Problems, Freiberg (Germany), Sept. 21-22, 2000, pp. 91-98
- [2] P. Fiser, and J. Hlavicka, Implicant Expansion Method used in the BOOM Minimizer. Proc. IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS'01), Gyor (Hungary), 18-20.4.2001, pp. 291-298
- [3] J. Hlavicka, and P. Fiser, A Heuristic method of two-level logic synthesis. Proc. The 5th World Multiconference on Systemics, Cybernetics and Informatics SCI'2001, Orlando, Florida (USA) 22-25.7.2001, vol. XII, pp. 283-288
- [4] P. Fiser, and J. Hlavicka, On the Use of Mutations in Boolean Minimization. Proc. Euromicro Symposium on Digital Systems Design, Warsaw (Poland) 4-6.9.2001, pp. 300-307
- [5] J. Hlavicka, and P. Fiser, BOOM - a Heuristic Boolean Minimizer. Proc. ICCAD-2001, San Jose, Cal. (USA), 4.-8.11.2001 (accepted for publication)
- [6] <http://cs.felk.cvut.cz/~fiserp/boom/>
- [7] R.K. Brayton et al., Logic minimization algorithms for VLSI synthesis. Boston, MA, Kluwer Academic Publishers, 1984
- [8] O. Coudert, Two-level logic minimization: an overview. Integration, the VLSI journal, 17-2, pp. 97-140, Oct. 1994
- [9] G.D.Hachtel and F. Somenzi, Logic synthesis and verification algorithms. Boston, MA, Kluwer Academic Publishers, 1996, 564 pp.
- [10] L. Jozwiak and A. Chojnacki, Effective and Efficient FPGA Synthesis through Functional Decomposition Based on Informational Relationship Measures, Proc. Euromicro Symposium on Digital Systems Design, Warsaw (Poland) 4-6.9.2001 pp.30-37
- [11] C. Scholl: Multi-output functional decomposition with exploitation of don't cares. Proc. DATE 98, pp743-748