Notes on the ISCAS'89 Benchmark Circuits

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MCNC, October 1989

The ISCAS'89 benchmarks are a set of 31 digital sequential circuits. These benchmarks were distributed on tape to participants of the Special Session on Sequential Test Generation, Int. Symposium on Circuits and Systems, May 1989, and are partially characterized in F. Brglez, D. Bryan, K. Kozminski in "Combinational Profiles of Sequential Benchmark Circuits", Proc. IEEE Int. Symposium on Circuits and Systems, pp. 1929-1934, May 1989. A reprint of the article is available with the tape from MCNC. Each circuit is described in two files: a generic gate-level netlist and a list of equivalence-collapsed faults. A simple translator is included to read/write the netlist. There are no schematic diagrams.

The article provides the following information about the benchmarks:

- circuit function (if known) and various circuit parameters
- random pattern testability in full scan mode
- sizes of tested, redundant and aborted faults in full scan mode
- an example of the generic netlist format
- examples of modelling options for the D-flipflops
- description of the simple fault collapsing algorithm used
- an example of a synthesized benchmark

Important note:
Since we use only the generic D-flipflop in the netlist, it is up to the user conducting the experiment to augment the flipflop with a set/reset pin or scan-in/scan-out pin. Without the additional controlling and observation pins, some portions of these circuits may be hard to initialize, control and observe.

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