Implicit Representations in Test Patterns
Compression for Scan-Based Digital Circuits

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Abstract—Current test generation and compression processes still have room for improvement. One important factor is the representation of test vector sets that a tool uses internally. We overview known approaches to this problem, and present our results with implicit representation by instances of the satisfiability problem.

Keywords: Test compression, testing, implicit representation

I. INTRODUCTION
With the growing complexity of designs, the amount of test patterns need to be stored and applied grows up significantly. That is why the compression of test patterns is needed to decrease the memory requirement and time consumption of the test.

ATPG (Automatic Test Pattern Generator) and compression of test patterns for combinational (or full-scan) circuits is based on manipulation with sets of binary vectors. The sets express the possibilities of choice (at least one vector from the set is needed) or summary (the whole set of vectors is needed). Such sets can be expressed explicitly, as an enumeration of vectors, or implicitly, by describing the required characteristic properties of the set.

II. PREVIOUS WORK
The most frequently formalism for implicit characterization is the incompletely specified Boolean function. It cannot, however, describe any set of vectors. Therefore, while incompletely specified functions can improve size, the description remains partially explicit. Moreover, representations such as Binary Decision Diagrams [28] or And Inverter Graphs [29] are difficult to extend to incompletely specified functions.

III. IMPLICIT REPRESENTATIONS IN TEST COMPRESSION
Our aim is to develop a better compression method for RESPIN [27] and similar architectures. Compression in this case is based on overlapping the test patterns; therefore it requires choosing the right patterns in the right order to ensure optimum compression.

We realized that the set of patterns detecting a fault can be naturally and compactly described by an instance of satisfiability problem (SAT) as it is done in SAT-based ATPG [24, 25]. Furthermore, additional constraints can be easily added to the instance, selecting suitable patterns from the set.

Our tool, SAT Compress [33] uses such constraints to make sure that an overlap with previously generated data is possible. This allows us to generate only suitable vectors, and generate them in the process of compression. The core algorithm is a simple greedy procedure, accepting the first vector that can be overlapped.

A comparison of compressed test lengths in bits for seven different state-of-the-art compression techniques and SAT-Compress are presented in Table I. Even with such a simple method we can obtain similar results such as these state-of-the-art compression methods and in some cases even better. The run time is longer, however, we are aware that test time and not test generation time is the bottleneck.

IV. FUTURE WORK
The existing algorithm and tool harness the basic benefits from the implicit characterization. However, generating, storing and handling the SAT instances can be much improved. The efficiency could then translate into a more thorough heuristic process, giving good results more consistently.

In farther view, RESPIN and the overlapping compression can be replaced with another decompressor, more compatible with SAT description.

V. CONCLUSION
The test vector representation influences substantially the architecture of test compress tools. The advantages of implicit representation by SAT instances are documented on a compression tool for the RESPIN architecture.
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REFERENCES


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<th>TABLE I.</th>
<th>COMPARISON OF THE TEST DATA SIZE FOR DIFFERENT COMPRESSION TECHNIQUES</th>
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<tbody>
<tr>
<td>Bench. circuits</td>
<td>MinTest</td>
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<tr>
<td>s5378</td>
<td>20,758</td>
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<tr>
<td>s9234</td>
<td>25,935</td>
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<td>s13850</td>
<td>58,656</td>
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<td>s35932</td>
<td>21,156</td>
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<tr>
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<td>113,152</td>
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<td>s38584</td>
<td>161,040</td>
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