DDECS

DESIGN & DIAGNOSTICS of ELECTRONIC CIRCUITS & SYSTEMS

25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems DDECS 2022

April 6–8, 2022
Prague, Czech Republic


Invitation
OSCILLOSCOPE DAYS 2022
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Online Event
27th – 28th April 2022
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Embedded Technologies for a Safe & Secure connected Future

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- Increase awareness about PikeOS
- Increase amount of people having hands-on expertise with PikeOS
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- Introductory guest lectures
- PikeOS labs at universities
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- Research Project Manager

Research Areas

include (and are not limited to):

Operating Systems

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Networking

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DESIGN & DIAGNOSTICS of ELECTRONIC CIRCUITS & SYSTEMS

DDECS

25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems DDECS 2022

The International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS) provides a forum for exchanging ideas, discussing research results, and presenting practical applications in the areas of design, test, and diagnosis of microelectronic digital, analog, and mixed-signal circuits and systems.

General information

Conference venue

Hotel Diplomat Prague
Czech Technical University in Prague
Evropska 15, 160 41 Prague 6,Czech Republic

Local organizers

Czech Technical University in Prague is one of the biggest and oldest technical universities in Europe. It was founded on the initiative of Josef Christian Willenberg on the basis of a decree issued on January 18th, 1707 by Emperor Josef I.

Faculty of Information Technology has been established as the eighth faculty of the Czech Technical University in Prague on 1st July 2009.

CTU CZECH TECHNICAL UNIVERSITY IN PRAGUE

FACULTY OF INFORMATION TECHNOLOGY CTU IN PRAGUE

Committee

Organizing committee

General Chair
Hana Kubátová, CTU in Prague, CZ

General Vice Chair
Andreas Steininger, TU Vienna, AT

Program Chair
Maksim Jenihhin, TalTech, EE

Program Vice-chair
Tomasz Garbolino, Silesian UT, PL

Organizing Chair
Petr Fišer, CTU in Prague, CZ

Publication Chairs
Jan Bělohoubek, CTU in Prague, CZ
Jaroslav Borecký, CTU in Prague, CZ

Topic Chairs

Viera Stopjaková, STU, Bratislava, Slovakia: Analog, Mixed Signal, RF and Sensors

Miloš Krstić, IHP and University Potsdam, DE: Digital Circuit and System Design

Görschwin Fey, TU Hamburg, DE: Test, Verification and Dependability

Nele Mentens, KU-Leuven, BE: Secure HW and Embedded Systems

Oliver Keszöcze, FAU Erlangen-Nüremberg, DE: Emerging Technologies and New Computing Paradigms

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Accompanying program

April 6, 2022 | WEDNESDAY

Welcome Drink
Conference venue, Hotel Diplomat

April 7, 2022 | THURSDAY

Sightseeing Tour of Prague & Conference Dinner
walking tour with English speaking guides

17.00 Departure from the conference venue (Hotel Diplomat).

Places of interest:

1 – Prague castle stop – Start point of the tour (~17.30)

2 – Prague Castle

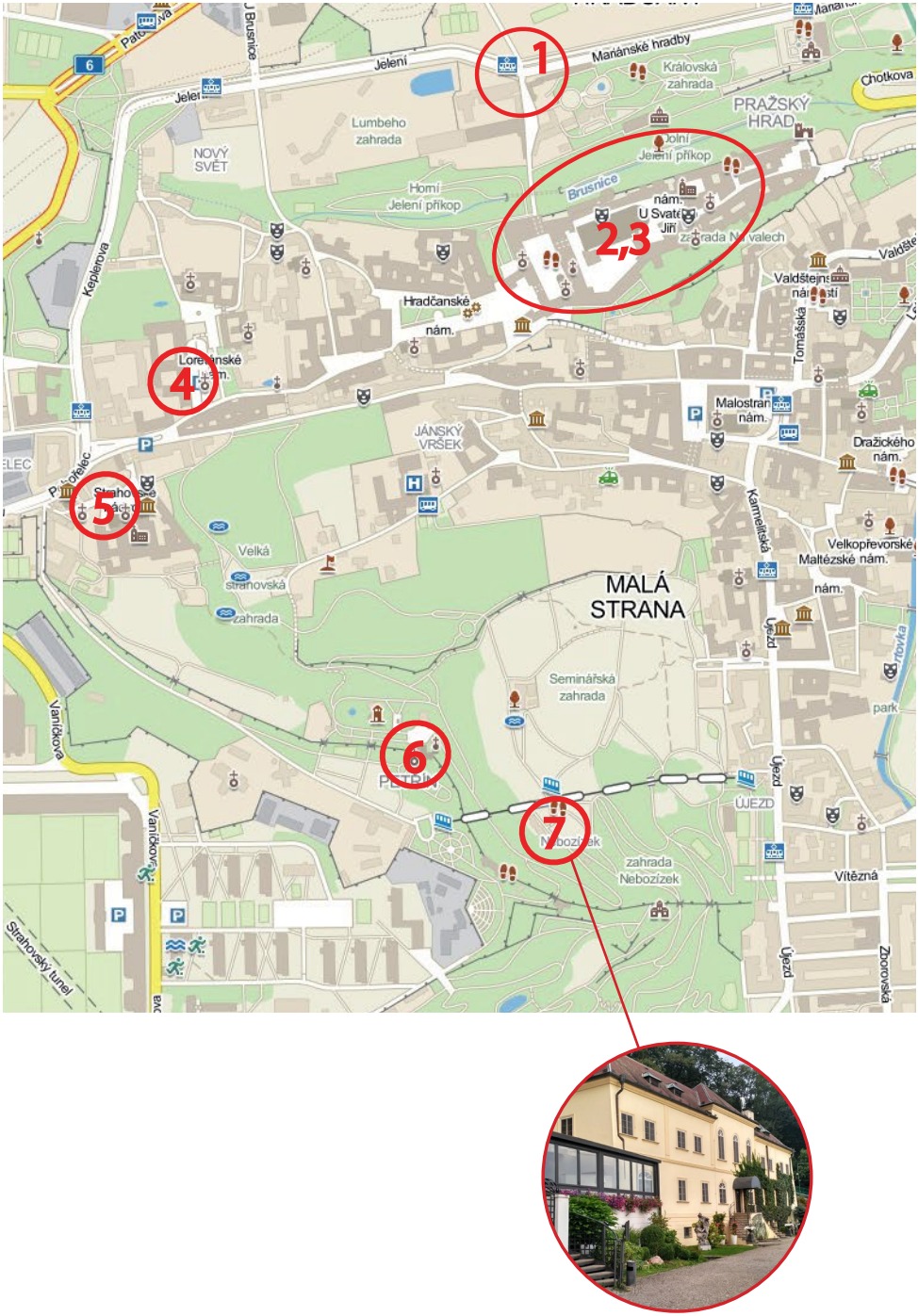
3 – Cathedral of St. Vitus at Prague Castle

4 – Czernin Palace

5 – Strahov Monastery

6 – Petřín Lookout Tower

7 – Restaurant Nebozízek (~19.00)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Dražického nám.
Malostranské nám.
Keplerova
Chotkova
park
Strahovský tunel

Scientific program

Wednesday, April 6, 2022

9:00–9:30 **Opening session**
Hana Kubátová, Petr Fišer, FIT, CTU in Prague, Czech Republic

9:30 Keynote lecture
Session chair: Hana Kubátová
A New Role of Design for Test in Silicon Lifecycle Management
Janusz Rajski, Siemens

10:15 Industrial talk
Session chair: Hana Kubátová
Experiences building a P4 Compiler for FPGAs
Pavel Benáček, Intel

10:45–11:00 Coffee break

11:00–12:15 Session 1: RISC Processors
Session chair: Miloš Krstić

- **Virtual Prototype driven Design, Implementation and Evaluation of RISC-V Instruction Set Extensions**
  Milan FUNCK[1], Vladimir HERDT[1,2], Rolf DRECHSLER[1,2]
  [1]DFKI GmbH, Germany; [2]University of Bremen, Germany

- **Early Performance Estimation of Embedded Software on RISC-V Processor using Linear Regression**
  Weiyan ZHANG[1], Mehran GOLI[1,2], Rolf DRECHSLER[1,2]
  [1]DFKI GmbH, Germany; [2]University of Bremen, Germany

- **Processor Extensions for Hardware Instruction Replay against Fault Injection Attacks**
  Noura AIT MANSSOUR[1,3], Vianney LAPOTRE[2,3], Guy GOGNIAT[2,3], Arnaud TISSERAND[1,3]
  [1]UBS, Lab-STICC, France; [2]Université Bretagne Sud; [3]CNRS, Lab-STICC, France

12:15–13:15 Lunch break

13:15 Embedded Tutorial
Session chair: Maksim Jenihhin

Hardware-Aware Neural Architecture Search
Lukáš Sekanina, VUT Brno, Czech Republic

14:15–15:20 Session 2: Novel Computing Architectures
Session chair: Maksim Jenihhin

- **AμFLIPS: An Asynchronous Microprocessor With FLexIbly-timed Pipeline Stages**
  Zaheer TABASSAM[1], Syed Rameez NAQVI[2], Andreas STEININGER[1]
  [1]TU Wien, Austria; [2]CUI, Wah Campus, Pakistan

- **A Design Space Exploration Framework for Memristor-Based Crossbar Architecture**
  Mario BARBARESCHI[1], Alberto BOSIO[2], Ian O'CONNOR[2], Petr FIŠER[3], Marcello TRAIOLA[4]
  [1]Department of Electrical Engineering and Information Technology, University of Naples Federico II, Naples, Italy; [2]Univ Lyon, ECL, INSA Lyon, CNRS, UCBL, CPE Lyon, INL, UMR5270, 69130 Ecully, France; [3]Czech Technical University in Prague, Czech Republic; [4]University of Rennes, Inria, CNRS, IRISA, UMR6074

- (S) **ArithsGen: Arithmetic Circuit Generator for Hardware Accelerators**
  Jan KLHUFEK, Vojtech MRAZEK, Brno University of Technology, Czech Republic

15:20–16:20 Posters (Regular), Coffee break

P1 **Fault Tolerant Synchronous Multi-Channel Buck Converter for Nuclear Inspection Instruments**
Yannick VERBELEN, Antonios BANOS, Tom B. SCOTT
University of Bristol, United Kingdom

P2 **Hardware Accelerated FrodoKEM on RISC-V**
Patrick KARL, Tim FRITZMANN, Georg SIGL, Technical University of Munich, Germany

P3 **Equivalence Checking of System-Level and SPICE-Level Models of Linear Analog Filters**
Kemal Çağlar COŞKUN, University of Bremen, Germany

P4 **ML-based Power Estimation of Convolutional Neural Networks on GPGPUs**
Christopher A. METZ[1], Mehran GOLI[1,2], Rolf DRECHSLER[1,2]
[1]Institute of Computer Science, Universität Bremen, Germany; [2]Cyber-Physical Systems, DFKI Bremen, Germany

P5 **On the optimization of Software Obfuscation against Hardware Trojans in Microprocessors**
Luca CASSANO[1], Elia LAZZERI[1], Nikita LITOVCHENKO[1], Giorgio DI NATALE[2]
[1]Politecnico di Milano, Italy; [2]Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA, France

16:20–17:40 **Session 3: Analog and Mixed-Signal Design**
Session chair: Viera Stopjaková

- **Hexapod Robotic System for Indoor Neutron and Gamma Radiation Mapping and Inspection**
  Antonis BANOS, Yannick VERBELEN, Suresh KALUVAN, Chris HUTSON, Matthew RYAN TUCKER, Tom B. SCOTT, University of Bristol, United Kingdom

- **Autocalibration Approach for Improving Robustness of Analog ICs**
  David MALJAR, Daniel ARBET, Martin KOVÁČ, Róbert ONDICA, Viera STOPJAKOVÁ, Slovak University of Technology, Slovak Republic

- (S) **A Radiation Tolerant CML Voltage-Controlled Oscillator in 65 nm CMOS**
  Jaime Sebastian CARDENAS CHAVEZ[1], Cheng GU[1], Zhi Chao ZHANG[1], Riu CHEN[1], Hormoz DJAHANSHAH[2]
  [1]University of Saskatchewan, Canada; [2]Microchip Technology

- (S) **On-Chip Current Sensing Approaches for DC-DC Converters**
  Richard RAVASZ, Adam HUDEC, Daniel ARBET, Viera STOPJAKOVÁ, Slovak University of Technology, Slovak Republic

18:30 **Welcome drink**

Thursday, April 7, 2022

9:00 Keynote lecture
Session chair: Petr Fišer

Towards Polynomial Formal Verification of Complex Arithmetic Circuits
Rolf Drechsler, University of Bremen, Germany

9:45 Industrial talk
Session chair: Petr Fišer

Safety-Critical Embedded Software Technology Innovations in Sysgo
Sysgo

10:15–10:30 Coffee break

10:30–11:50 Session 4: Hardware Security
Session chair: Martin Novotný

- **Hardware Obfuscation of Digital FIR Filters**
  Levent AKSOY[1], Alexander HEPP[2], Johanna BAEHR[2], Samuel PAGLIARINI[1]
  [1]Tallinn University of Technology, Estonia; [2]Technical University of Munich, Germany

- **Exploiting PUF Variation to Detect Fault Injection Attacks**
  Troya Cagil KOYLU, Luiza CAETANO GARAFFA, Cezar Rodolfo WEDIG REINBRECHT, Mahdi ZAHEDI, Said HAMDIOUI, Mottaqiallah TAOUIL
  Delft University of Technology, The Netherlands

- **Versatile Hardware Framework for Elliptic Curve Cryptography** (S)
  Vít MAŠEK, Martin NOVOTNÝ, Czech Technical University in Prague, Czech Republic

- **Correlation Power Analysis of SipHash** (S)
  Matúš OLEKŠÁK, Vojtěch MIŠKOVSKÝ, Czech Technical University in Prague, Czech Republic

11:50–13:00 Lunch break

13:00–14:00 **Panel Session: Secure hardware architectures and systems**
Moderator: Nele Mentens, Leiden University and KU Leuven, The Netherlands

Panelists

- Lejla Batina, Radboud University, The Netherlands
- Ahmad-Reza Sadeghi, TU Darmstadt, Germany
- Akash Kumar, TU Dresden, Germany
- Petr Svenda, Masaryk University, Brno, Czech Republic

14:00–14:15 *Coffee break*

14:15–15:45 **Special Session: Dependability of Alternative Computing Paradigms for Machine Learning: hype or hope?**
Session chair: Alberto Bossio

- **Memristive Logic-in-Memory Implementations: Benefits and Limitations**
  Giorgio Di Natale, CNRS/TIMA, France

- **Are SNNs Fault Tolerant?**
  Ioana Vatajelu, CNRS/TIMA, France

- **CNN Fault Tolerance: Myth and Reality**
  Luca Cassano, Politecnico di Milano, Italy

17:00 **Social Event**
Departure from the hotel, Sightseeing (walking) tour of Prague

Friday, April 8, 2022

9:30 Keynote lecture
Session chair: Nele Mentens

AI and Side-Channel analysis: Lessons Learned So Far
Lejla Batina, Radboud University, Nijmegen, The Netherlands

10:15–11:30 Session 5: Formal Verification
Session chair: Katarina Jelemenská

- **Analyzing Dynamic Aspects of AxC Systems by Means of Statistical Model Checking**
  Josef STRNADEL, Brno University of Technology, Czech Republic

- **Functional Verification of Arithmetic Circuits: Survey of Formal Methods**
  Maciej CIESIELSKI, Atif YASIN, Jiteshri DASARI
  University of Massachusetts, Amherst, MA, USA

- **On SAT-Based Model Checking of Speed-Independent Circuits**
  Florian HUEMER, Robert NAJVIRT, Andreas STEININGER
  Institute for Computer Engineering, TU Wien, Vienna, Austria

11:30–11:45 Coffee break

11:45–13:00 Session 6: Emerging Technologies and New Computing Paradigms
Session chair: Lukáš Sekanina

- **Synaptic Control for Hardware Implementation of Spike Timing Dependent Plasticity**
  Salah DADDINOUNOU, Elena-Ioana VATAJELU
  Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA, France

- **Programmable Logic Elements Using Multigate Ambipolar Transistors**
  Ashton SNELGROVE, Pierre-Emmanuel GAILLARDON, University of Utah, USA

- **A Concept Towards Pressure-Controlled Microfluidic Networks**
  Gerold FINK[1], Medina HAMIDOVIĆ[1], Werner HASELMAYR[1], Robert WILLE[2,3]
  [1]Johannes Kepler University Linz, Austria; [2]Technical University of Munich, Munich, Germany; [3]Software Competence Center Hagenberg GmbH (SCCH), Hagenberg, Austria

13:00–14:00 Lunch break

14:00–14:50 Session 7: Stochastic Computing
Session chair: Elena-Ioana Vatajelu

- **Stochastic Computing Architectures for Lightweight LSTM Neural Networks**
  Roshwin SENGUPTA[1], Ilia POLIAN[1], John P. HAYES[2]
  [1]University of Stuttgart, Germany; [2]University of Michigan, USA
- **Analyzing Multilevel Stochastic Circuits using Correlation Matrices**
  Owen S. HOFFEND, John P. HAYES, University of Michigan, USA

14:50–15:20 Posters (Informal), Coffee break

P6 **Scalable FPGA Hardware Accelerator for SVM Inference**
Marcin AFTOWICZ[1], Kai LEHNIGER[1], Peter LANGENDOERFER[1,2]
[1]IHP - Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany; [2]BTU CS - Brandenburg University of Technology Cottbus-Senftenberg, Germany

P7 **Identifying Critical Flip-flops in Circuits with Graph Convolutional Networks**
Li LU[1], Junchao CHEN[1,2], Markus ULBRICHT[1], Milos KRSTIC[1,2]
[1]IHP-Leibniz-Institut für innovative Mikroelektronik, Germany; [2]University of Potsdam, Potsdam, Germany

P8 **Verification of Calculations of Non-Homogeneous Markov Chains Using Monte Carlo Simulation**
Jan REZNICEK, Martin KOHLIK, Hana KUBATOVA
Czech Technical University in Prague, Czech Republic

15:20–16:10 Session 8: Reliability and Resilience of DNNs
Session chair: Giorgio Di Natale

- **Selective Hardening of Critical Neurons in Deep Neural Networks**
  Annachiara RUOSPO[1], Gabriele GAVARINI[1], Ilaria BRAGAGLIA[1], Marcello TRAIOLA[2], Alberto BOSIO[3], Ernesto SANCHEZ[1]
  [1]Politecnico di Torino, Italy; [2]Inria, University of Rennes, CNRS, IRISA, Rennes, France; [3]Univ Lyon, ECL, INSA Lyon, CNRS, UCBL, CPE Lyon, INL, UMR5270, France
- **Exploring Software Models for the Resilience Analysis of Deep Learning Accelerators: the NVDLA Case Study**
  Alessandro VERONESI[1], Francesco DALL'OCCO[2], Davide BERTOZZI[2], Michele FAVALLI[2], Milos KRSTIC[1,3]
  [1]IHP microelectronics, Germany; [2]University of Ferrara, Italy; [3]Universität Potsdam, Germany

16:10 **Closing**